Packaging Technology

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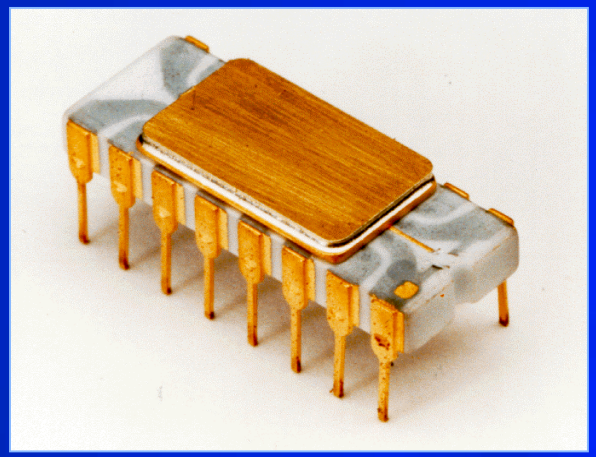
Assembly Technology Development
Intel Corporation

Agenda

- Packaging research @ Intel
- CPU package technology evolution snapshot
- Challenges ahead & our response
- Summary

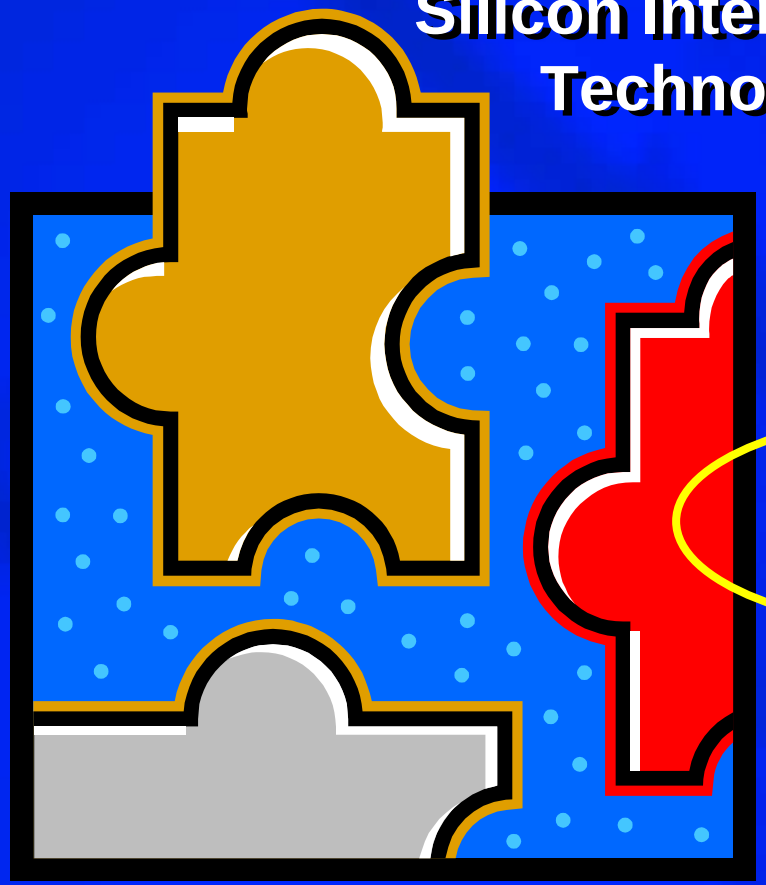
Microprocessors



1971

2002

Product success depends on …



Intel's Global Packaging Development

900+ people

* Also Intel Assembly and Test Site

Main R&D facility in Chandler, AZ

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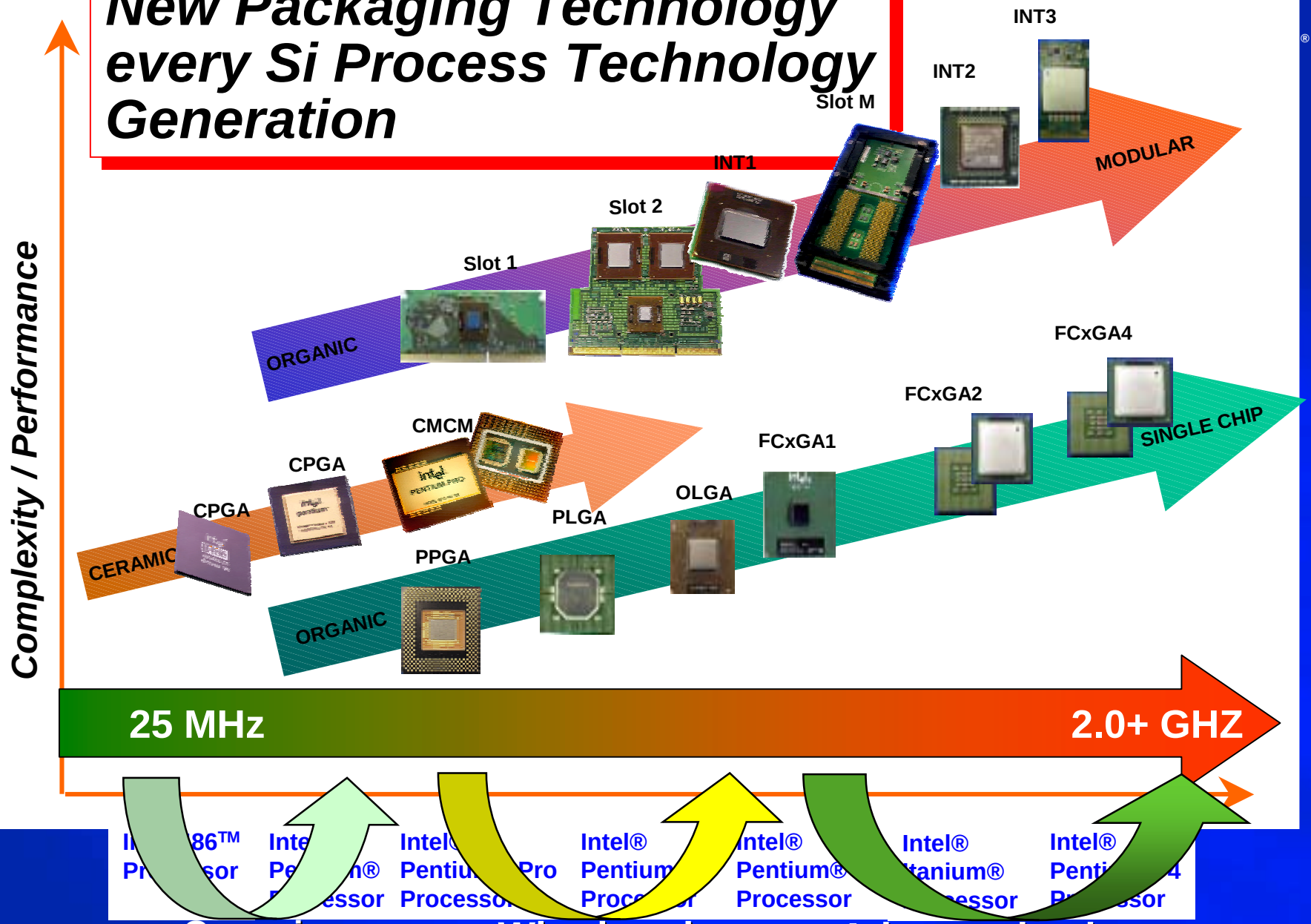
Packaging Technology Drivers

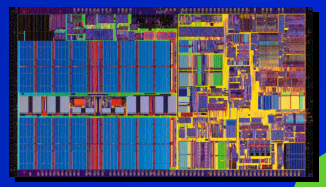
1. Silicon Technology advances
2. Product Performance Demands
3. Market Segmentation

Enable maximizing benefit from silicon technology and product advancements

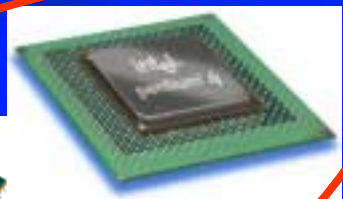
New Packaging Technology every Si Process Technology Generation

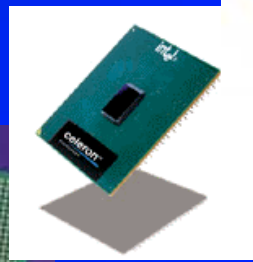


Custom solutions by market segment



Silicon Enabler





Value Add : custom solutions based on market segment

Agenda

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- **Challenges ahead & our response**
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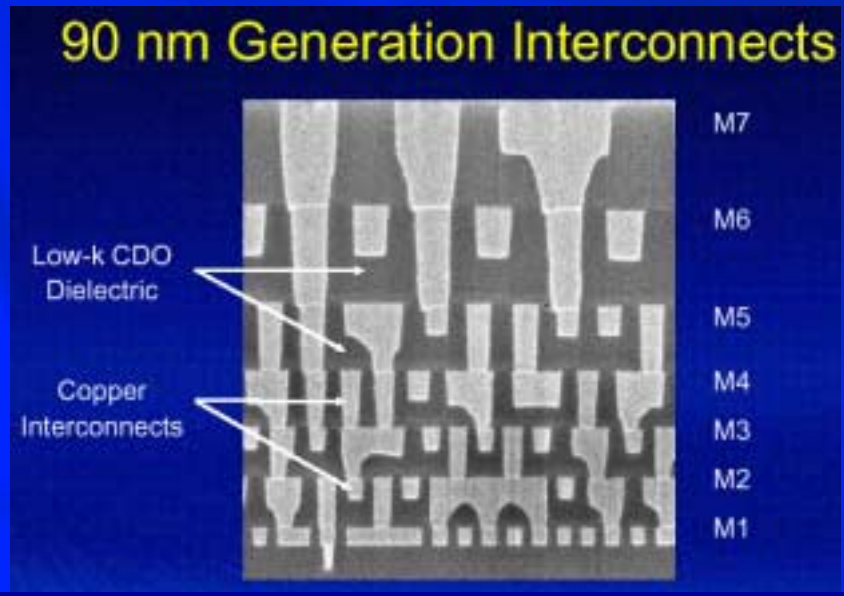
Challenges ahead

1. Silicon & Package integration becomes more complex
2. Interconnect scaling needs novel approaches
3. New package architecture for super fast processors
4. Cooling complexity increases
5. Wireless packaging trends
6. System-in-a-package
7. Lead free

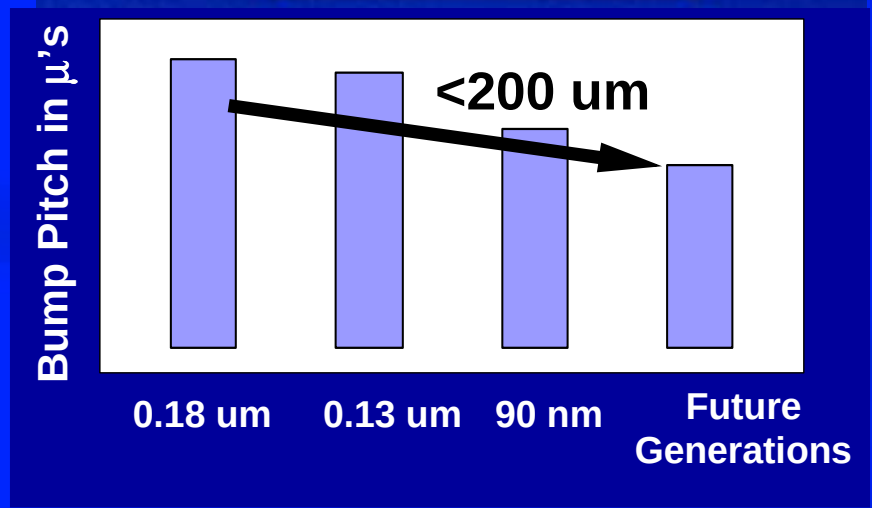
Goal : Bring technology innovation into High Volume Manufacturing at a LOW COST

Silicon + Package integration

- **Enabling Low-k / Ultra low-k dielectrics**
  - **Tuning pkg. substrate material set CTE (coefficient of thermal expansion) properties closer to silicon**



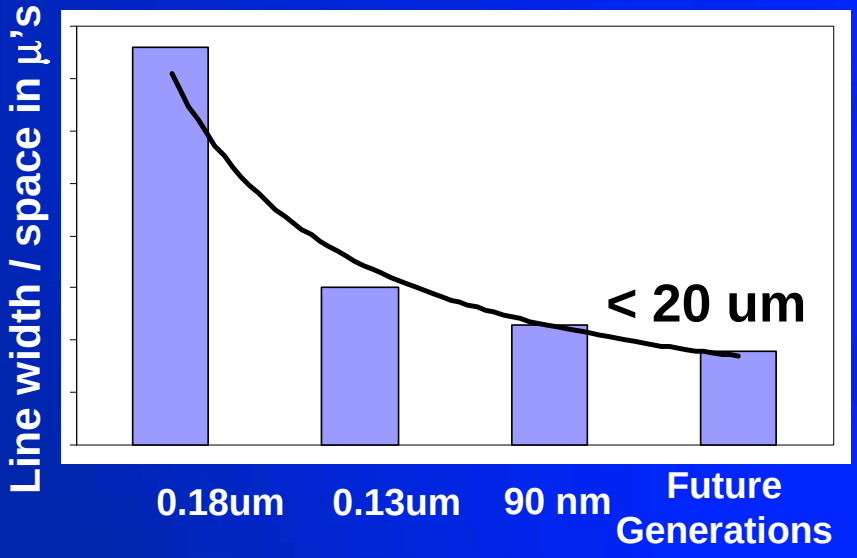
- **Enabling more flip chip bump connections and tighter bump pitch**
  - **Developing novel underfill processes**
  - **Equipment design / capability improvements**

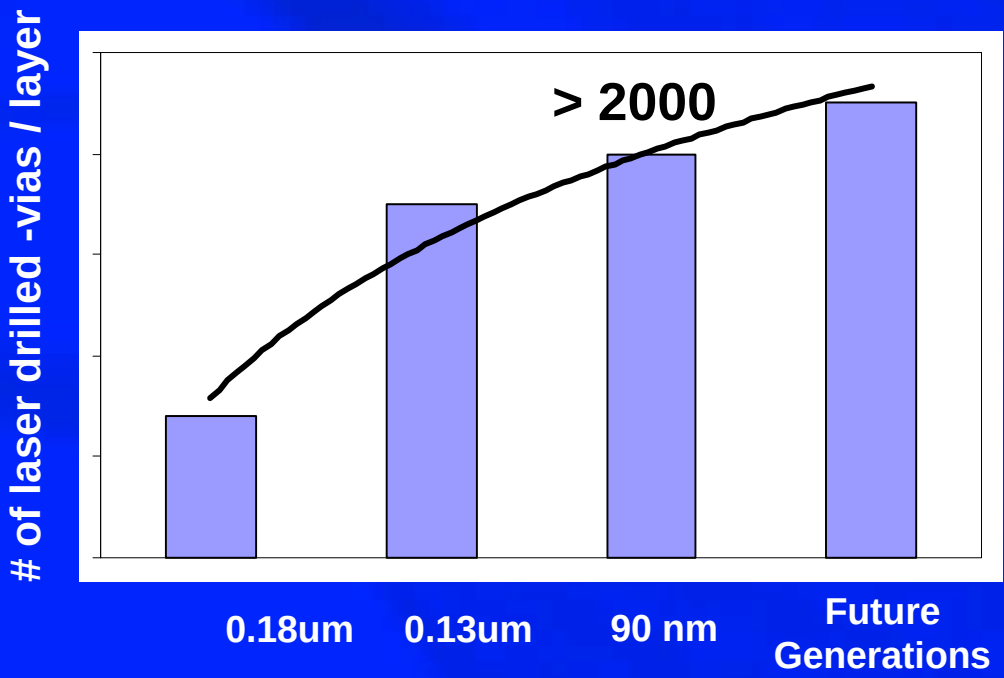


Source: Intel

Package Interconnect scaling

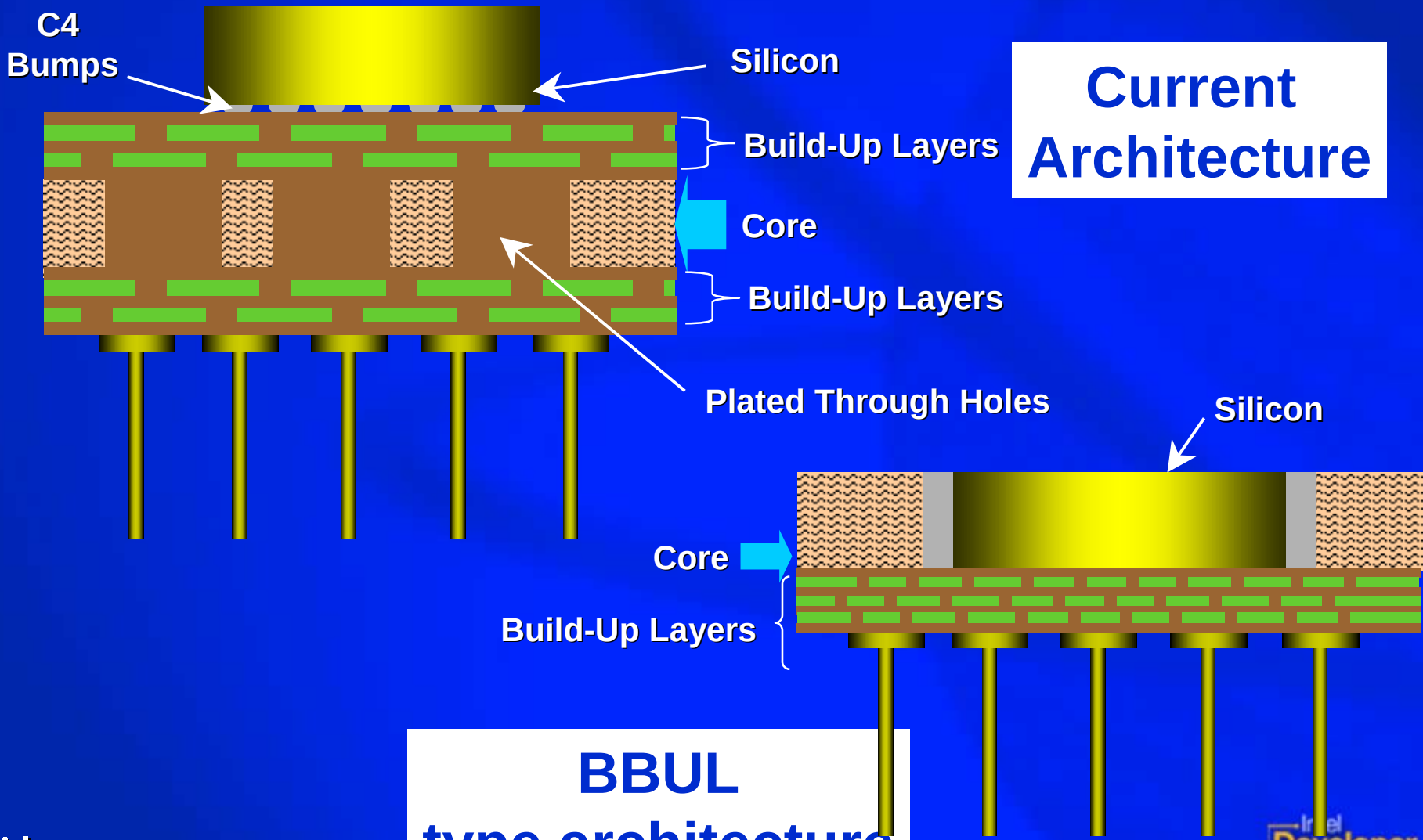
- **Traditional scaling methods approaching inflexion point**
  - **Fundamental research efforts underway to develop breakthrough interconnect solution (finer features @ even lower cost)**



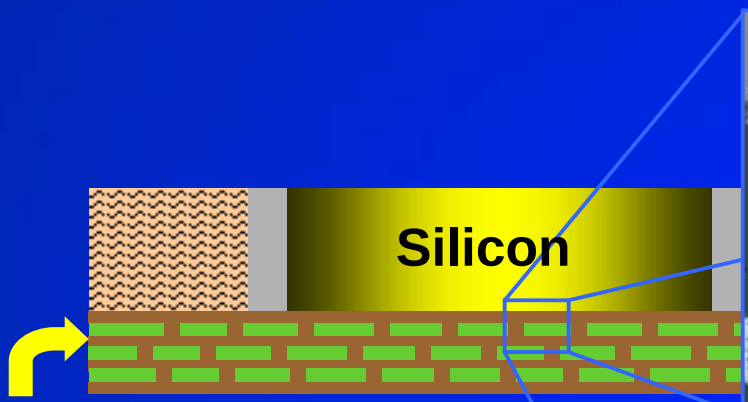


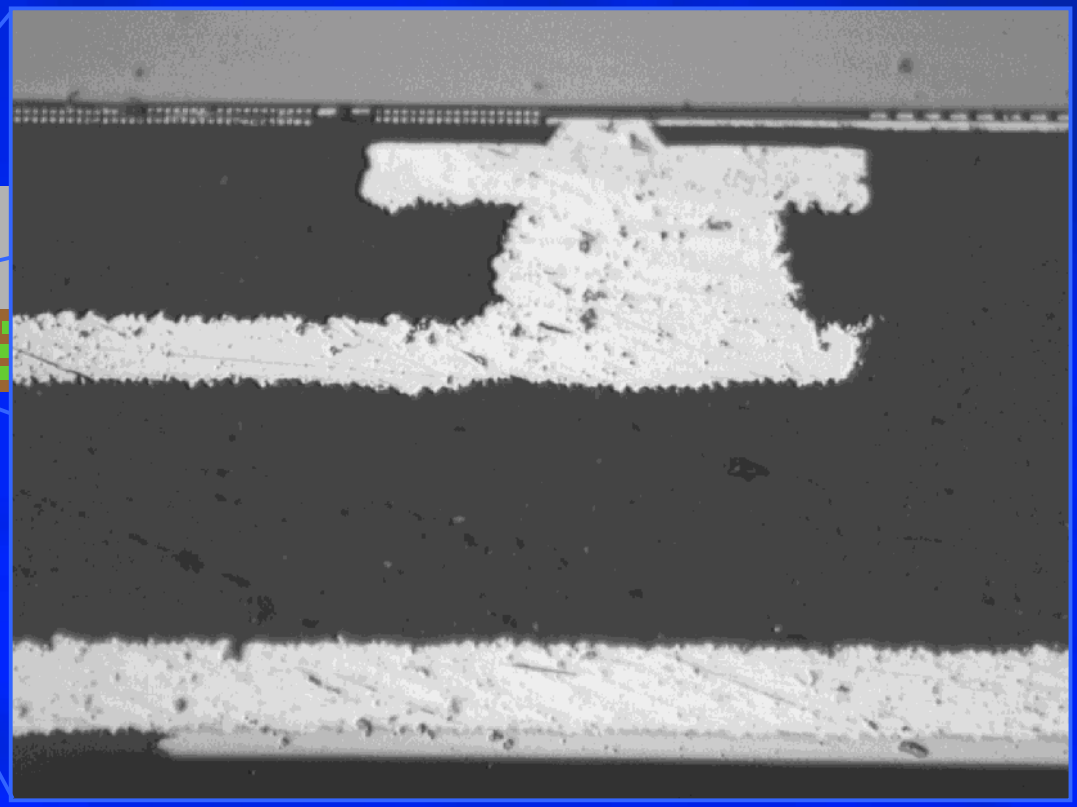
Source: Intel

New Architecture Concepts



BBUL Bump-less Build-Up Layer

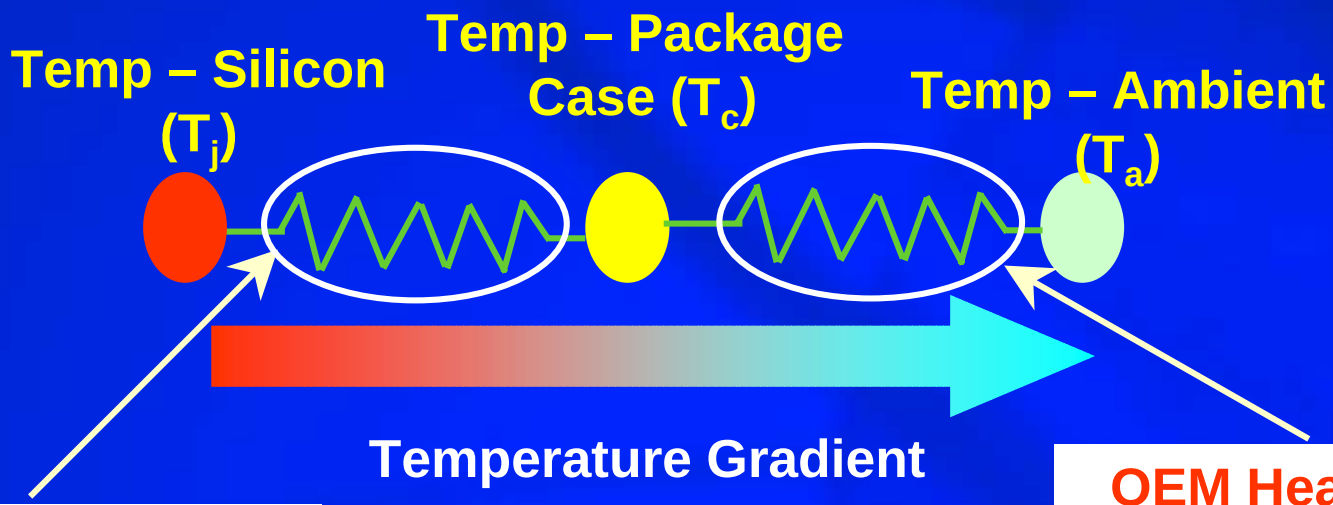




Thinner than a dime !

Cooling

Total Package + System Solution Thermal Budget

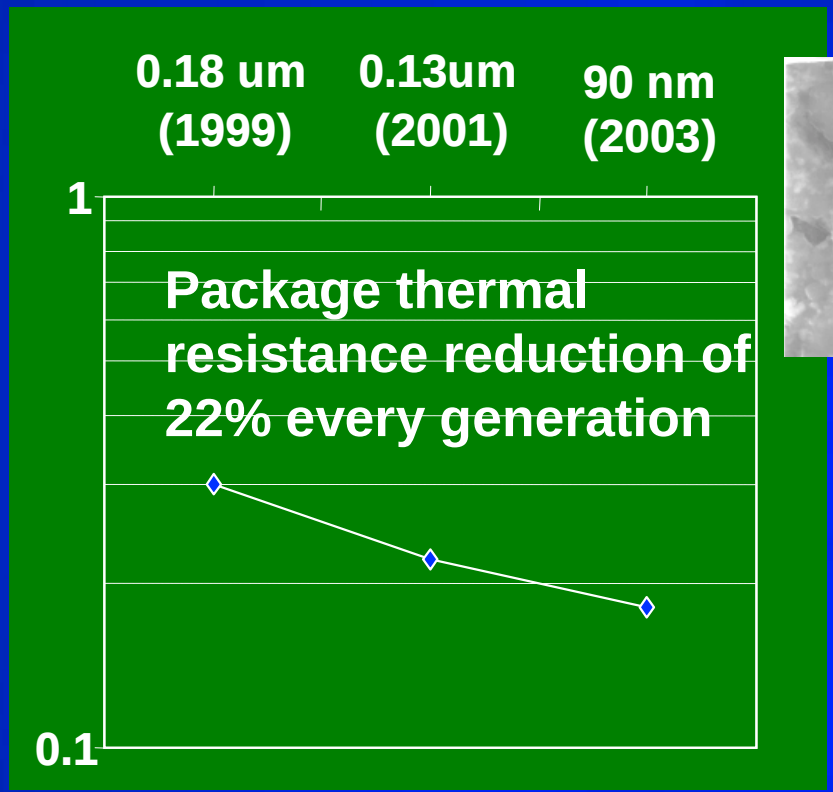


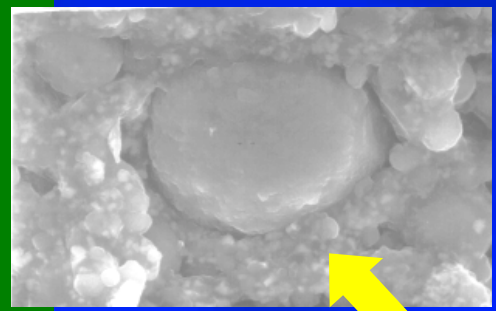
Packaging
Provide Solutions for this interface of the budget : Smooth out Hot Spots

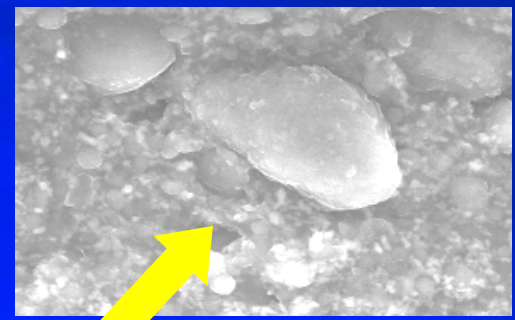
OEM Heat Sink
Provide Solutions for this interface of the budget

Integrated Thermal Solutions in the package reduce heat flux – easier to cool in the system

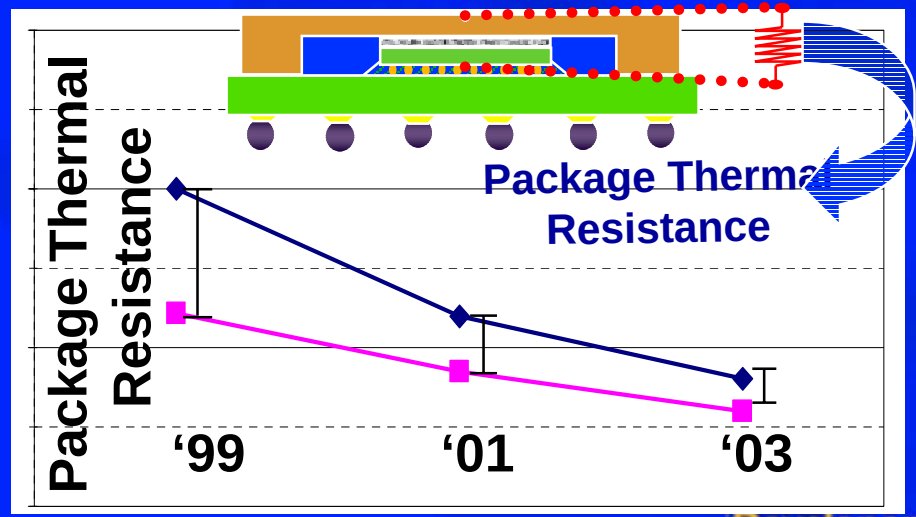
Advanced cooling capabilities







Adjusting filler particle geometry (regular vs. irregular) for TIMs to improve percolation



Source: Intel

Focus on fundamental materials formulation research & reducing process variability

Wireless Packaging Trends

- **Chip Scale Packaging**
  - **Pitch Reduction to .5mm (for the**
- **Memory and S**
  - **Stacked** **ckages coming**
- **, thin**
  - **00 µm die today to 75 µm die tomorrow**
- **High Volume**

Greater Performance, Memory, Computing in smaller mm³ space

System-in-a-Package Solutions:
Advanced Stacked CSP Technology

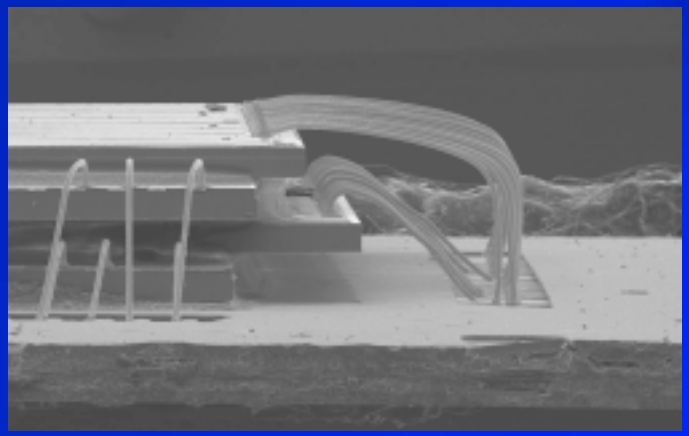
intel

Stacked Die

4 Die

3 Die

2 Die



4 Die Stack Sampling Now

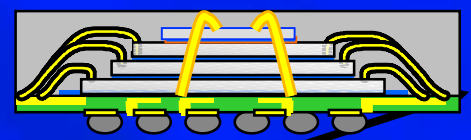
Intel has "The Right Stack"

More Die while getting Thinner

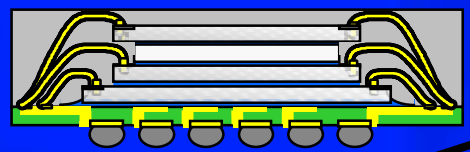
Reliable, Cost Effective

High Volume Assembly

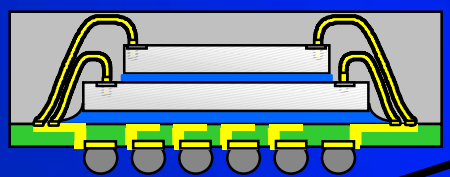
The System Solution



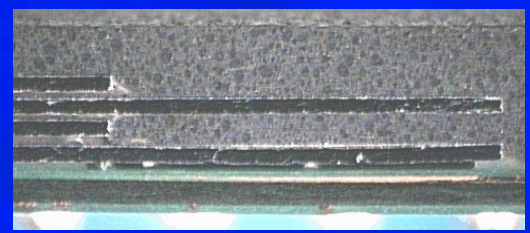
Sampling In 2002



Moving into Production



> 100 Million Shipped



Thin Is In… 3 mil or less die allows thinner packages

1.4mm Thick

1.2mm Thick

1.0mm Thick

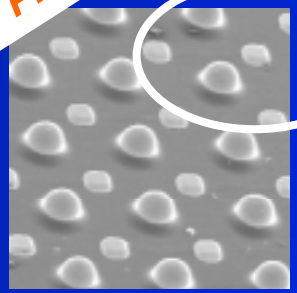
Intel Research & Development

Intel Developer Forum

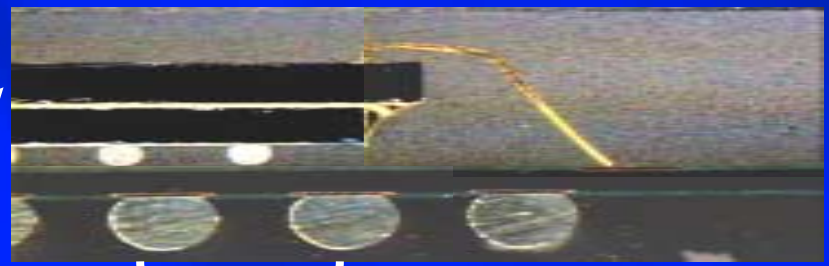
Flip Chip in CSPs

Flip Chip – 2002 Production

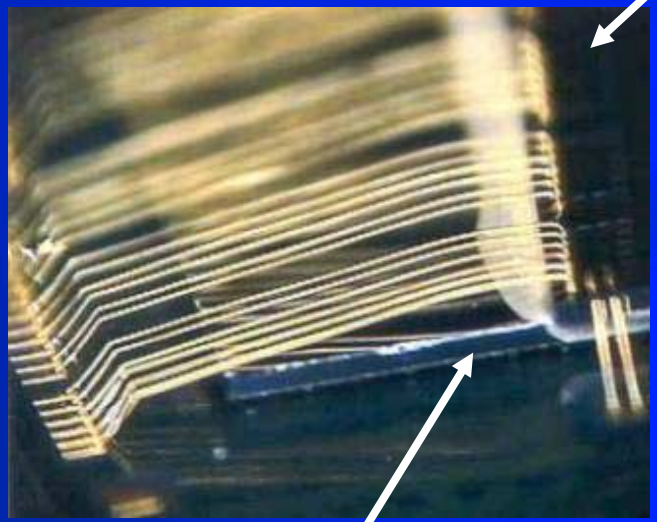
Array of Flip Chip Bumps on Chip



Stacked with
Wire Bonded Memory



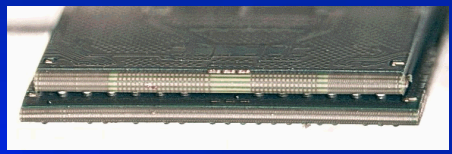
Package Solder Balls (.5mm pitch)

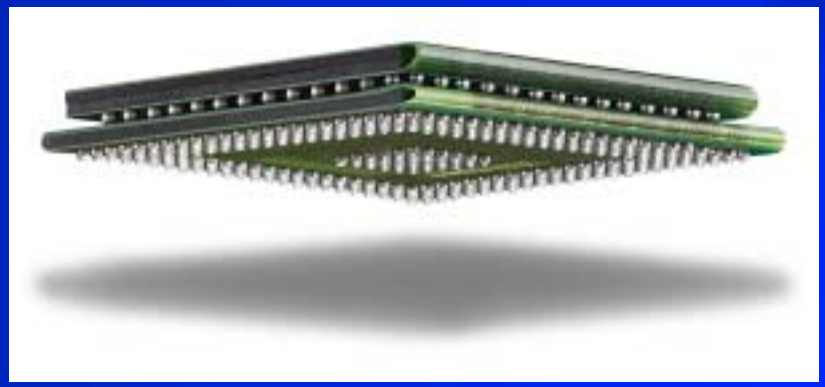


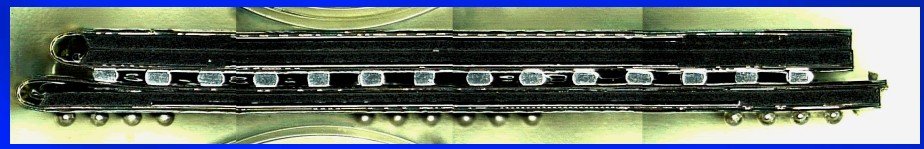
Flip Chip – Logic Device

- **Flip Chip Enables**
  - Higher frequencies
  - Reduction in package body size
  - Higher I/O in smaller chip area

The Ultimate Flexibility
Folded Stacked Packaging





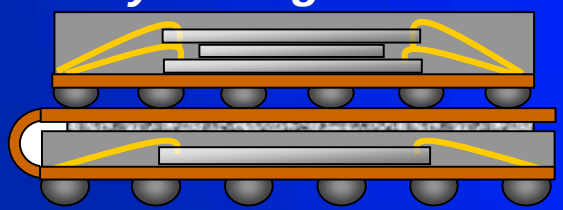


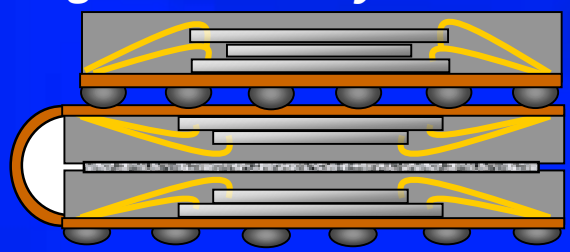
***World's First !!* - Folded Stacked CSP**

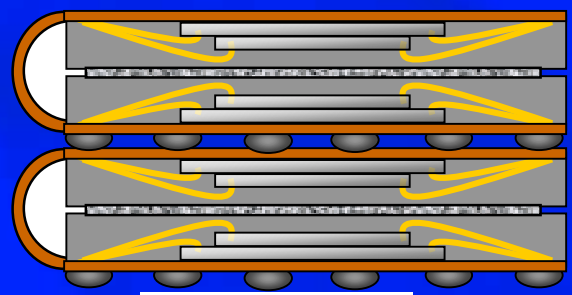
A system in Package

Sampling in 2002

Many Configurations of Logic & Memory Possible



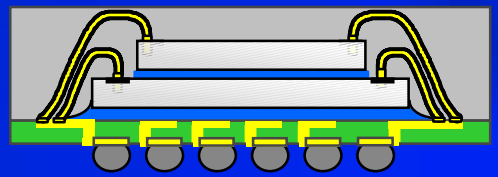




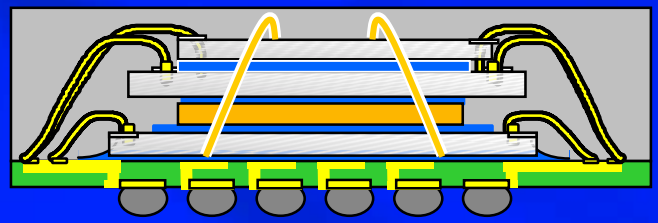
Animation

Logic - Memory System-in-a-Package

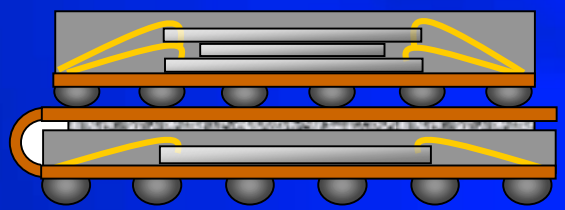
Several Flavors Being Developed



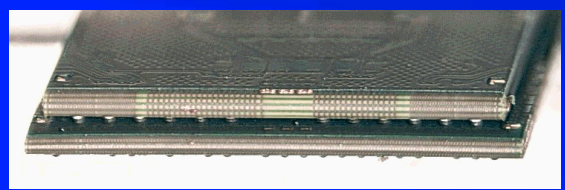
Wirebond Stacked CSP



Flip Chip/Wirebond Stacked CSP



Folded Stacked CSP



Lead Free - Where is Intel Today ?

- Intel's Commitment:
  - Dedicated significant resources to R&D for over 2.5 years
  - Develop lead-free solutions for package & board technologies
  - Develop lead-free solutions with the industry
  - New Updates: **http://www.intel.com/research/silicon/leadfree.htm**
- Intel's Performance:
  - Intel has successfully developed Pb-free package and process technology
    - Management of a flawless transition to Pb-free products is a major challenge for the industry
  - Range of lead-free technologies developed including:
    - Solder alloy selection (SnAgCu & Matte Tin), package and printed circuit board materials and manufacturing process
  - Working with industry consortia, suppliers and customers to establish compatible Pb-free solutions

CSP Package Technology Summary

- ***Significant New Technology*** **in CSP's Being Developed at Intel and moved into Assembly**
  - **Broad portfolio of Package options being developed**
  - **Discrete and stacked multichip/SIP Solutions**
  - **Implementing as required to support products**
  - **Reliable, cost effective, High Volume solutions**
  - **Lead Free**
- **Increasing silicon & package integration**
  - **Thinner, Higher Performance, Great Silicon Flexibility**
- **Leadership Package Technology**

In Summary ...

Key Messages

- **Innovation in packaging continues to be key to Intel's technology leadership**
- **Many new challenges emerging …**
  - **Silicon + packaging integration, breakthrough interconnect schemes, cooling, ultra-thin stacking solutions, chip scale packaging, lead free etc.**
- **We have plans & resources to address each of these challenges**
- **Intel's approach – integrated solutions from silicon ⇔ packaging ⇔ systems**

Thank You !

For more information, please visit ….

http://www.intel.com/research/silicon/packaging.htm

http://developer.intel.com/technology/itj/

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